

**Amendments to the Claims:**

This listing of claims replaces all prior versions, and listings, of claims in this application.

**Listing of Claims:**

1. (Currently Amended) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display mode;

a filter for processing said analog image signal and providing a processed image signal at an internal node; and

a clamping circuit connected between said internal node and a reference level;

wherein said filter provides a variable bandwidth in response to said display mode;

wherein said clamping circuit is used to clamp said processed image signal by said reference level during a clamping interval.

2. (Original) The interface circuitry as claimed in claim 1, wherein said filter comprises:

a variable resistor electrically connected between said input node and said internal node;

and

a capacitor electrically connected between said internal node and a ground node.

3. (Original) The interface circuitry as claimed in claim 1, wherein said clamping circuit comprises a transistor connected between said internal node and said reference level.

4. (Original) The interface circuitry as claimed in claim 3, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

5. (Original) The interface circuitry as claimed in claim 1, wherein said clamping circuit comprises:

a variable resistor connected to said internal node; and  
a transistor connected between said variable resistor and said reference level.

6. (Original) The interface circuitry as claimed in claim 5, wherein said transistor is configured with a drain connected to said variable resistor, a source connected to said reference level and a gate controlled by a clamping signal.

7. (currently amended) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display mode;  
a filter for processing said analog image signal and providing a processed image signal at an internal node;  
an ADC unit for converting said processed image signal into a digital image signal; and  
a clamping circuit connected between said internal node and a reference level;  
wherein said filter provides a variable bandwidth in response to said display mode;

wherein said clamping circuit is used to clamp said processed image signal by said reference level during a clamping interval.

8. (Original) The interface circuitry as claimed in claim 7, wherein said filter comprises:  
a variable resistor electrically connected between said input node and said internal node;  
and

a capacitor electrically connected between said internal node and a ground node.

9. (Original) The interface circuitry as claimed in claim 7, wherein said clamping circuit comprises a transistor connected between said internal node and said reference level.

10. (Original) The interface circuitry as claimed in claim 9, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

11. (Original) The interface circuitry as claimed in claim 7, wherein said clamping circuit comprises:

a variable resistor connected to said internal node; and  
a transistor connected between said variable resistor and said reference level.

12. (Original) The interface circuitry as claimed in claim 11, wherein said transistor is configured with a drain connected to said variable resistor, a source connected to said reference level and a gate controlled by a clamping signal.